AMENDMENTS TO THE CLAIMS:

1-2.   (Canceled)

3.   (Currently amended) The method according to claim ~~1~~ 40, wherein ~~said placement and~~ the netlist modification ~~transforms are~~ is divided into a set of steps, each step addressing a specific ~~phase~~ aspect of the ~~placement and synthesis process~~ design space.

4.   (Canceled)

5.   (Currently amended) The method according to claim ~~1~~ 40, wherein ~~a single sequence of sets of steps of the transforms~~ the modification optimizes the combination of the physical, Boolean and electrical ~~domains, thus moving the design from a start point to an end point in the design space~~ domains.

6.   (Currently amended) The method according to claim ~~1~~ 40, wherein ~~a single sequence of sets of steps of the transforms~~ the modification affects multiple objectives and constraints which involve physical placement, electrical properties, and logical data.

7-11.   (Canceled)

12.   (Currently amended) The method according to claim ~~1~~ 40 , further comprising:
at predetermined stages of the ~~process~~ method, selectively determining whether to intercept the ~~process~~ method and implement ~~any of a plurality of transforms~~ the most recently considered netlist modification and cell placement.

13. (Currently amended) The method according to claim ~~1~~ 40, further comprising:

examining a plurality of domains to find an improved design, said examining

comprising ~~creating a sequence of steps of placement and netlist~~ evaluating the effects of the

considered netlist modification ~~transforms, to create a design closure process meeting~~ and cell

placement on design performance targets.

14-23. (Canceled)

24. (Currently amended) The system according to claim ~~22~~ 46, wherein ~~said placement and~~

the netlist modification ~~transforms are~~ is divided into a set of steps, each step addressing a

specific ~~phase~~ aspect of the ~~placement and synthesis process~~ design space.

25. (Canceled)

26. (Currently amended) The system according to claim ~~22~~ 46, wherein ~~a single set of steps~~

~~of the transforms~~ the modification optimizes the combination of the physical, Boolean and

electrical ~~domains, thus moving the design from a start point to an end point in the design space~~

domains.

27. (Currently amended) The system according to claim ~~22~~ 46, wherein ~~a single set of steps~~

~~of the transforms includes multiple objectives and constraints which affect~~ the modification

affects physical placement, electrical properties, and logical data.

28-32. (Canceled)

33.   (Currently amended) The system according to claim 22 46, further comprising:

a unit for selectively determining, at predetermined stages of the process, whether to intercept the process and implement any of a plurality of transforms the most recently considered netlist modification and cell placement.

34.   (Currently amended) The system according to claim 22 46, further comprising:

an examining unit for examining a plurality of domains to find an improved design, said examining unit comprising a unit for creating a sequence of steps of placement and evaluating the effects of the considered netlist modification transforms, to create a design closure process meeting and cell placement on design performance targets.

35-39. (Canceled)

40.   (New) A method of modifying a plurality of domains of a circuit in a design space, the domains including at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprising a plurality of cells, said method comprising:

(a) considering a possible netlist modification for the design space;

(b) considering a cell placement for the modified netlist;

(c) determining whether the considered netlist modification and the considered cell placement improve the design space; and

(d) if the considered netlist modification and the considered cell placement improve the design space, implementing the considered netlist modification and the considered cell placement, but if the considered netlist modification and the considered cell placement do not improve the design space, returning to (a).

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41.   (New) The method according to claim 40, wherein considering a cell placement comprises considering a plurality of placement techniques.

42.   (New) The method according to claim 40, wherein the design space is divided into bins, and (a) through (c) are performed on a bin.

43.   (New) The method according to claim 40, wherein (c) further comprises determining whether further improvement of the design space should be sought; and, if so, returning to (a).

44.   (New) The method according to claim 40, further comprising making an initial layout for the design space.

45.   (New) The method according to claim 40, further comprising storing information to update data about the implemented netlist and cell placement.

46.   (New) A system for modifying a plurality of domains of a circuit in a design space, the domains including at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprising a plurality of cells, said system comprising:

    (a) a unit for considering a possible netlist modification for the design space;

    (b) a unit for considering a cell placement for the modified netlist; and

    (c) a unit for determining whether the considered netlist modification and the considered cell placement improve the design space.

47.   (New) The system according to claim 46, further comprising a unit for implementing the considered netlist modification and the considered cell placement.

48.   (New) The system according to claim 46, further comprising a unit for making an initial layout for the design space.

49.   (New) The system according to claim 46, further comprising a unit for storing data about the implemented netlist and cell placement.

50.   (New) A programmable storage medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to modify a plurality of domains of a circuit in a design space, the domains including at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprising a plurality of cells, said method comprising:

(a) considering a possible netlist modification for the design space;

(b) considering a cell placement for the modified netlist;

(c) determining whether the considered netlist modification and the considered cell placement improve the design space; and

(d) if the considered netlist modification and the considered cell placement improve the design space, implementing the considered netlist modification and the considered cell placement, but if the considered netlist modification and the considered cell placement do not improve the design space, returning to (a).

51.   (New) The programmable storage medium according to claim 50, wherein considering a cell placement comprises considering a plurality of placement techniques.

52.   (New) The programmable storage medium according to claim 50, wherein the design

space is divided into bins, and (a) through (c) are performed on a bin.

53.   (New) The programmable storage medium according to claim 50, wherein (c) further comprises determining whether further improvement of the design space should be sought; and, if so, returning to (a).

54.   (New) The programmable storage medium according to claim 50, wherein the method further comprises making an initial layout for the design space.

55.   (New) The programmable storage medium according to claim 50, wherein the method further comprises storing information to update data about the implemented netlist and cell placement.